Digital Gate Driver IC with Fully Integrated Automatic Timing Control Function in Stop-and-Go Gate Drive for IGBTs

Dibo Zhang, Kohei Horii, Katsuhiro Hata, and Makoto Takamiya
The University of Tokyo, Tokyo, Japan

***Abstract*— To reduce loss and noise during switching of IGBTs at low cost even under changing operating conditions, namely load current (I_L) and junction temperature (T_J) variation, the world's first active digital gate driver IC with fully integrated automatic timing control function that achieves both single-chip integration and real-time control is developed. In order to handle various IGBTs with one type of gate driver, the proposed IC also has the world's first 6-bit programmable gate current function in the closed-loop active gate drivers. In the double pulse test of IGBT, compared with the conventional single-step gate drive, the stop-and-go gate drive with automatic timing control using the proposed IC effectively reduces the switching loss (E_{LOSS}) under the collector current overshoot ($I_{OVERSHOOT}$)-aligned condition and reduces $I_{OVERSHOOT}$ under E_{LOSS}-aligned condition with I_L ranging from 10 A to 80 A and T_J ranging from 25 ˚C (room temperature) to 125 ˚C, and particularly at the condition of I_L = 80 A at 25 ˚C, the proposed gate driver reduces E_{LOSS} by 49 % under the $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 33 % under the E_{LOSS}-aligned condition.**

***Keywords*— IGBT, IC, surge current, energy loss, active gate driver**

I. Introduction

A lot of active gate drivers (AGDs), where the gate driving waveform is controlled during the turn-on/off transients, have been proposed to reduce both the switching loss and the switching noise of power devices. AGDs can be classified into two types, open-loop control [1-6] and closed-loop control [7-19, 22]. The closed-loop AGDs are required instead of the open-loop AGDs, because the optimal driving waveform changes depending on the operating conditions (e.g. load current and temperature) [20]. Fig. 1 summarizes the design choices in conventional closed-loop AGDs. To make the closed-loop AGDs practical, the following three points are required: (1) single-chip integration instead of PCB implementation for lower cost, (2) real-time control instead of iterative control to reliably handle dynamic change of operating conditions, and (3) programmable AGDs instead of fixed-function AGDs that require individual optimization for different product variety of power devices. In the closed-loop AGDs, however, no previous paper has realized (1) and (2) simultaneously, and no previous paper on (3) has been published. To solve the problems, in this paper, a digital gate driver (DGD) IC with fully integrated automatic timing control (ATC) function for IGBTs that realizes all of (1) to (3) is proposed. The design choices in this paper are shown in blue in Fig. 1.

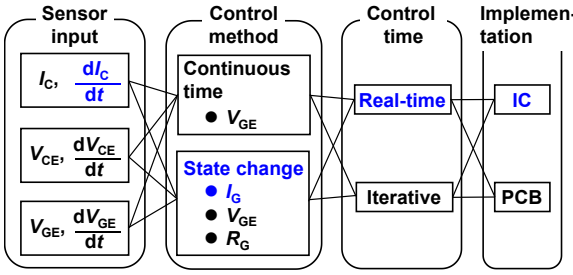


Fig. 1: Design choices in closed-loop AGDs. This work is shown in blue.

II. Proposed Digital Gate Driver IC with Automatic Timing Control

Figs. 2 and 3 show a circuit schematic and a timing chart of the proposed DGD IC with ATC, respectively. In the following, turn-on is discussed, whereas the exact same is true for turn-off. The IC includes dI_C/dt detector for the state change, controller for ATC, and a 6-bit current-source type

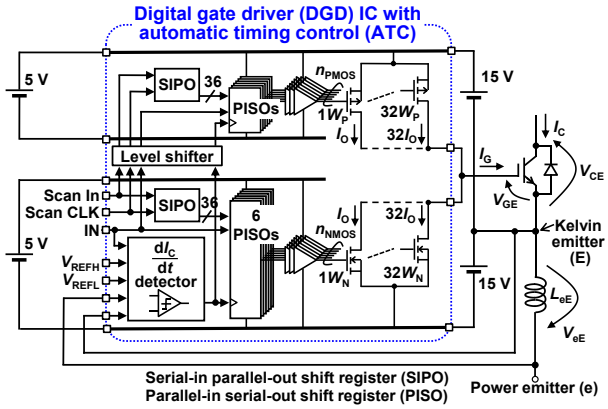


Fig. 2: Circuit schematic of proposed DGD IC with ATC.

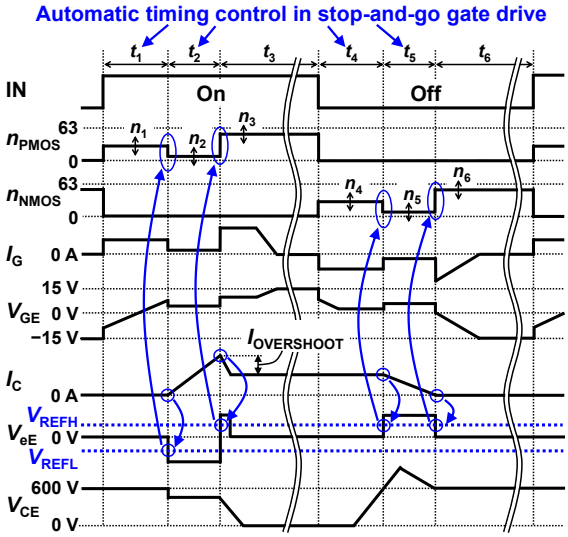


Fig. 3: Timing chart of proposed DGD IC with ATC.

digital gate driver with variable gate current (I_G) in 64 levels, where $I_G = n_{PMOS} \times 48$ mA and n_{PMOS} is an integer from 0 to 63 (max I_G = 3A). At turn-on, an active gate driving is performed in three slots from t_1 to t_3 with different I_G of strong (n_1) -weak (n_2) -strong (n_3), and this driving method is defined as stop-and-go gate drive (SGGD) [21]. I_G switching is realized by a digital timing control input from dI_C/dt detector to parallel-in serial-out registers (PISO) to drive nMOSFETs and pMOSFETs with different gate widths connected in parallel. n_1 to n_3 are preset by a digital input (Scan In), while t_1 and t_2 are automatically determined by ATC. An important feature of this IC is the full integration of t_1 and t_2 real-time automatic control functions on a single chip. The real-time control of t_1 and t_2 is done by detecting dI_C/dt by sensing the voltage (V_{eE}) of the parasitic inductance (L_{eE}) between Kelvin emitter and power emitter in Fig. 2, because $V_{eE} = -L_{eE}(dI_C/dt)$, where I_C is the collector current. Specifically, as shown in Fig. 3, the end timing of t_1 is determined by detecting the negative V_{eE} at the beginning of I_C flow using a comparator with the reference voltage of V_{REFL}, and the end timing of t_2 is determined by detecting the positive V_{eE} at the timing immediately after I_C overshoots using a comparator with the reference voltage of V_{REFH}. Similarly, at turn-off, t_4 to t_6 is also automatically switched by the comparing the reference voltage with V_{eE} completed by dI_C/dt detector.

Fig. 4 shows a die photo of DGD IC with ATC fabricated with 180-nm BCD process. The die size is 2.0 mm by 2.5 mm.

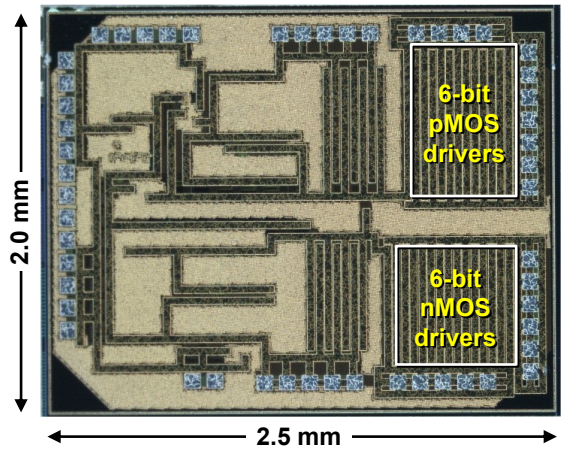


Fig. 4: Die photo of DGD IC with ATC.

III. Measured Results

Figs. 5 and 6 show a circuit schematic and a measurement setup of the double pulse test using the developed DGD IC and an IGBT module (FS100R12N2T4, 1200 V, 100 A), respectively. The IGBT module is placed on a hotplate for measurement under different temperature. In this paper, only turn-on measurements are discussed, and turn-off measurements are not discussed, because, in the IGBT module, no trade-off relationship between the turn-off loss and the collector-to-emitter voltage overshoot was observed when I_G of DGD IC was varied.

Figs. 7 (a) and (b) show the timing charts for turn-on of the conventional single-step gate drive (SSGD) and the proposed SGGD for comparison, respectively. In SSGD, n_1 is varied from 4 to 63, which emulates a conventional gate driver with varied gate resistance. In SGGD, on the other hand, (n_1, n_2, n_3) are preset to (40, 0, 63), a set of parameters where

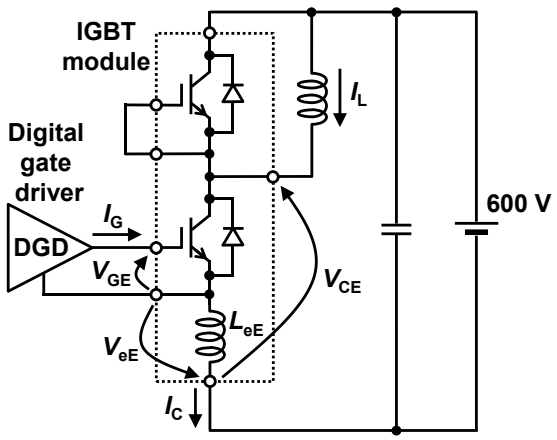


Fig. 5: Circuit schematic of double pulse test.

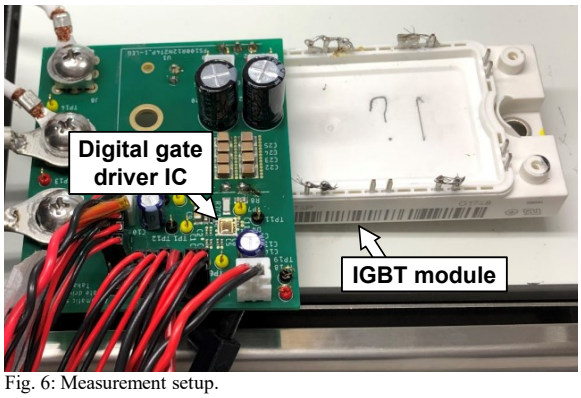


Fig. 6: Measurement setup.

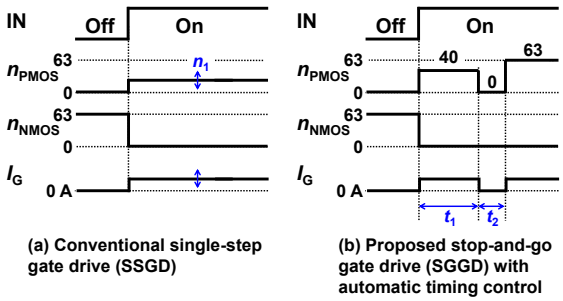


Fig. 7: Timing charts for turn-on.

$I_{OVERSHOOT}$ is optimally suppressed with the weakest driving forced "0", and follow-up turning-on is returned with the greatest driving force "63" to maximumly reduce further energy loss, and t_1 and t_2 are automatically determined by ATC.

Figs. 8 (a) to (c) show the measured I_C and Figs. 8 (d) to (f) show the gate-emitter voltage (V_{GE}) waveforms in SGGD with ATC with varied load current (I_L) from 10 A to 80 A, and junction temperature (T_J) of 25 ˚C, 75 ˚C (IC average temperature 60 ˚C), and 125 ˚C (IC average temperature 90 ˚C), respectively. V_{GE} waveforms explicitly show the sunken parts, which represent t_2, varied in duration corresponding to variation in I_L for each of the three T_J's measured, and t_1 remains the same within each T_J. Fig. 9 shows the measured t_2 vs. I_L relationship of the three sets of data in different T_J. t_2 is automatically increased by ATC, and it is clearly observed that as t_2 increases approximately linearly with I_L when T_J is

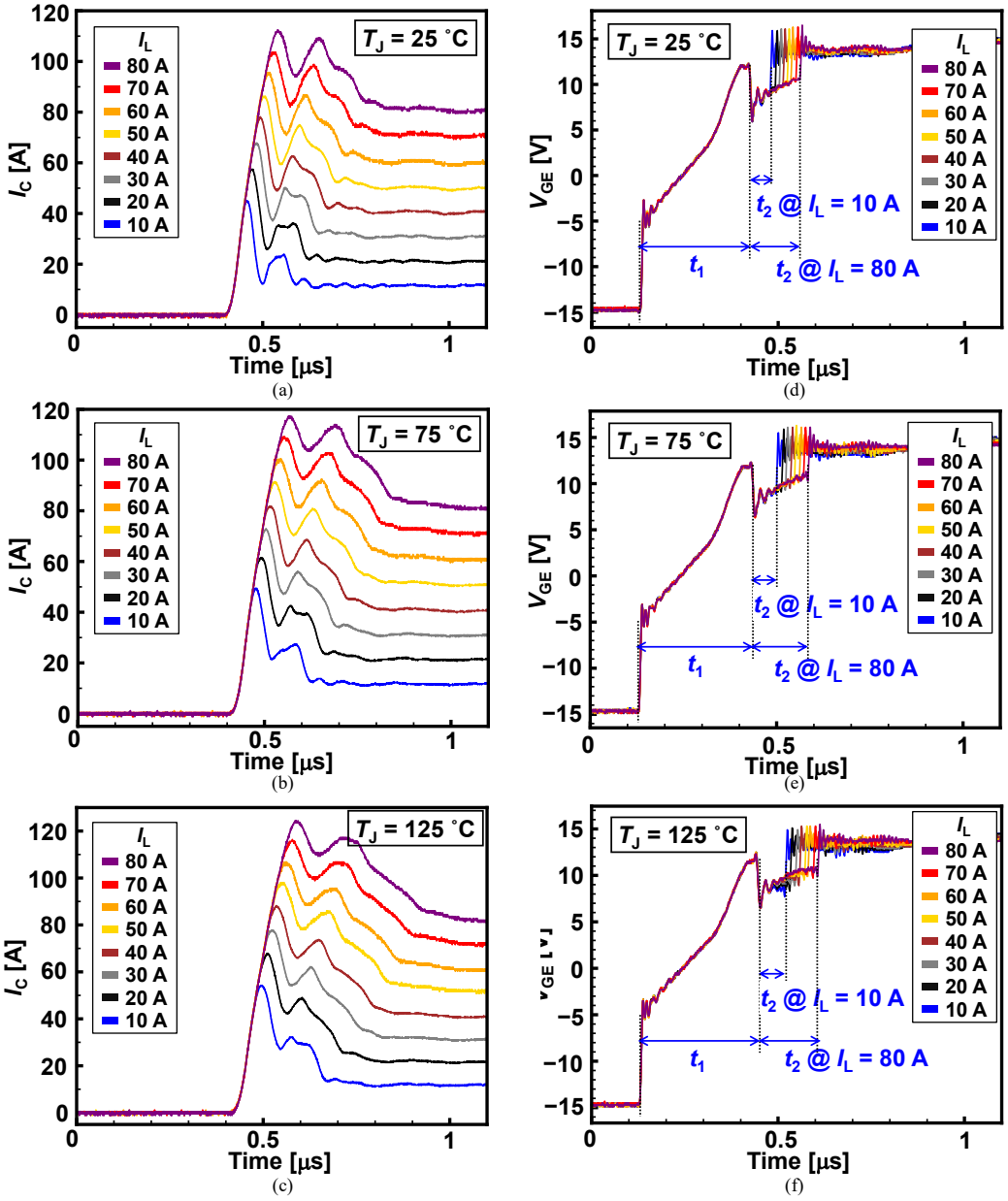


Fig. 8: Measured results in SGGD with ATC with varied I_L and T_J. (a) to (c) are I_C waveforms. (d) to (f) are V_{GE} waveforms. (a) and (d) for T_J = 25 ˚C. (b) and (e) for T_J = 75 ˚C. (c) and (f) for T_J = 125˚C.

the same. On the other hand, for a fixed I_L, t_2 duration increases as T_J increases, because according to the characteristics of the IGBT module under test, $I_{OVERSHOOT}$ increases as T_J increases. Therefore, the proposed gate driver automatically extend the weaker driving slot (t_2) to suppress the surge current.

Figs. 10 (a) to (c) show the measured switching loss (E_{LOSS}) vs. the collector current overshoot ($I_{OVERSHOOT}$) of the conventional SSGD and the proposed SGGD at I_L = 20 A, 50 A, and 80 A, respectively. In each graph, T_J is varied to 25 ˚C, 75 ˚C, and 125 ˚C. The red curve, which represents T_J = 125 ˚C, black curve, which represents T_J = 75 ˚C, and blue curve, which represents T_J = 25˚C, show the trade-off curves of the conventional SSGD with varied n_1 from 4 to 63. In all cases, the proposed SGGD has lower E_{LOSS} and lower $I_{OVERSHOOT}$

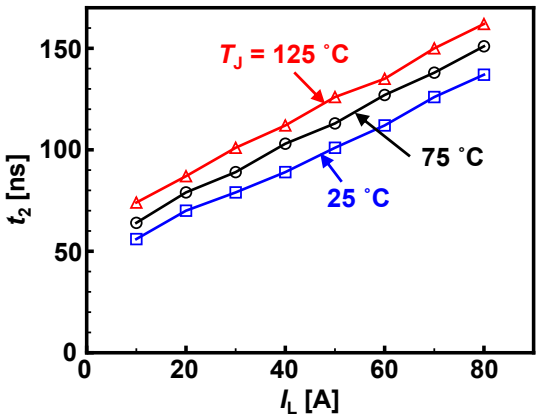
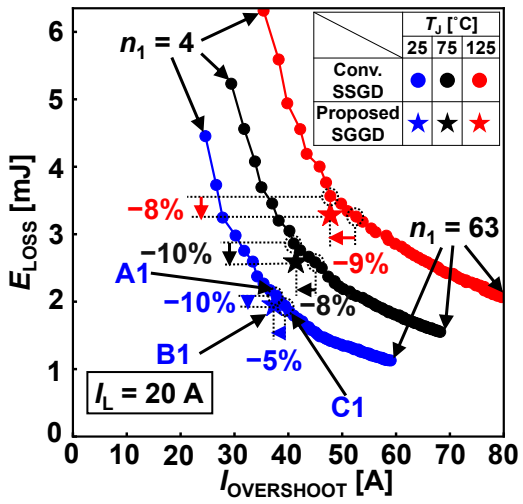
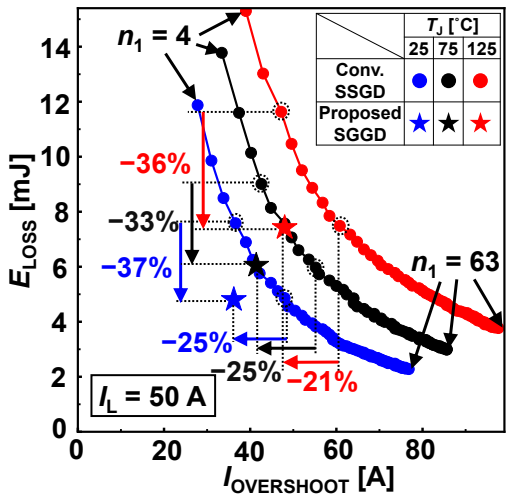


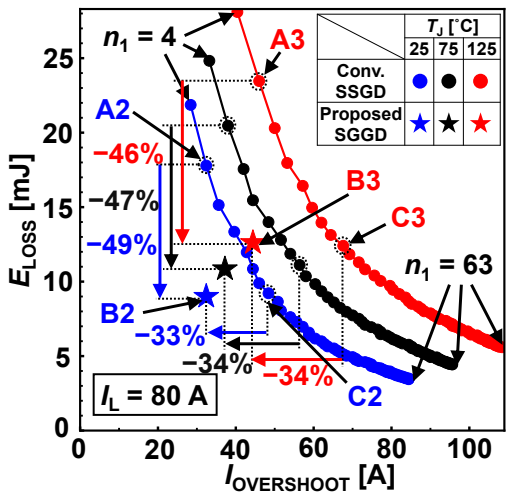
Fig. 9: Measured t_2 vs. I_L at T_J = 25 ˚C, 75 ˚C, and 125˚C.



(a)

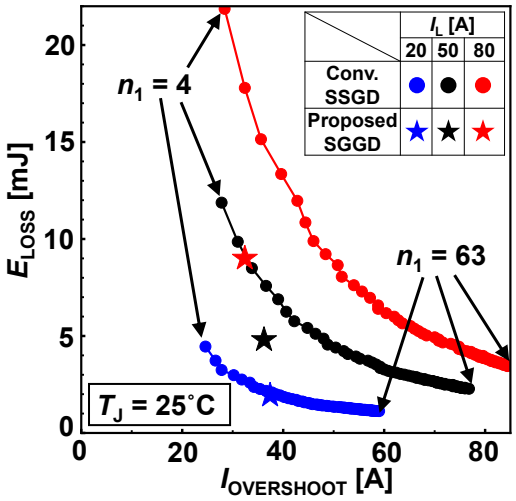


(b)

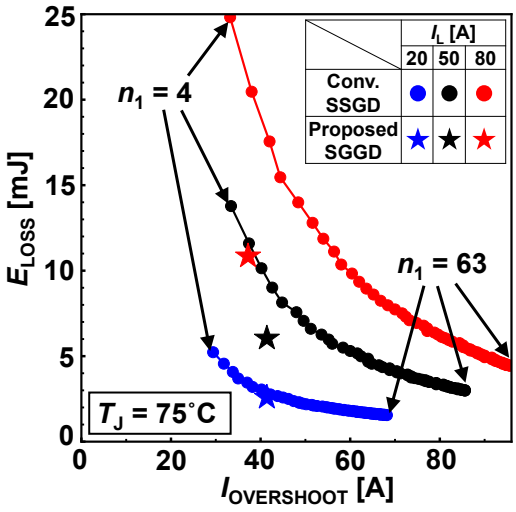


(c)

Fig. 10: Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SSGD and proposed SGGD at I_L = 20 A (a), 50 A (b), and 80 A (c), and each varies in T_J. Points A1 to A3, Points B1 to B3, and Points C1 to C3 are defined in (a) and (c).



(a)



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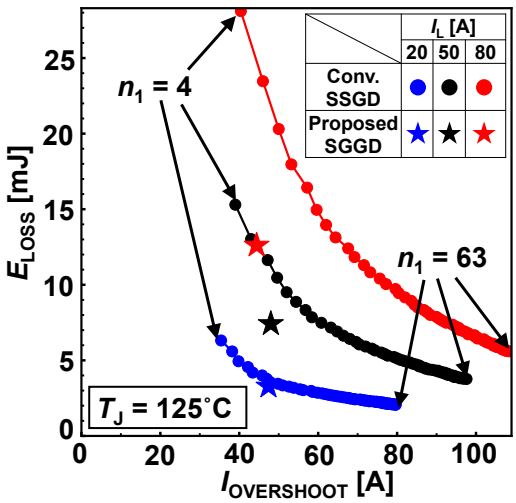

(c)

Fig. 11: Measured E_{LOSS} vs. $I_{OVERSHOOT}$ of conventional SSGD and proposed SGGD at T_J = 25 °C (a), 75 °C (b), and 125 °C (c), and each varies in I_L.

than the conventional SSGD. In Figs. 10 (a) and (c), Points A1 to A3, Points B1 to B3, and Points C1 to C3 are defined for (I_L, T_J) = (20 A, 25 ˚C), (80 A, 25 ˚C), and (80 A, 125 ˚C), respectively, where Points "B"s are the proposed SGGD, Point "A"s are the conventional SSGD with closest $I_{OVERSHOOT}$ comparing to proposed ones, and Point "C"s are the conventional SSGD with the closest E_{LOSS} comparing to proposed ones. The measured waveforms for these nine points are shown later in Figs. 12 to 14. At (I_L, T_J) = (20 A, 25 ˚C) in Fig. 10 (a), compared with the conventional SSGD (Point A1 and Point C1), the proposed SGGD (Point B1) reduces E_{LOSS} by 10 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 5 % under E_{LOSS}-aligned condition. At (I_L, T_J) = (80 A, 25 ˚C) in Fig. 10 (c), compared with the conventional

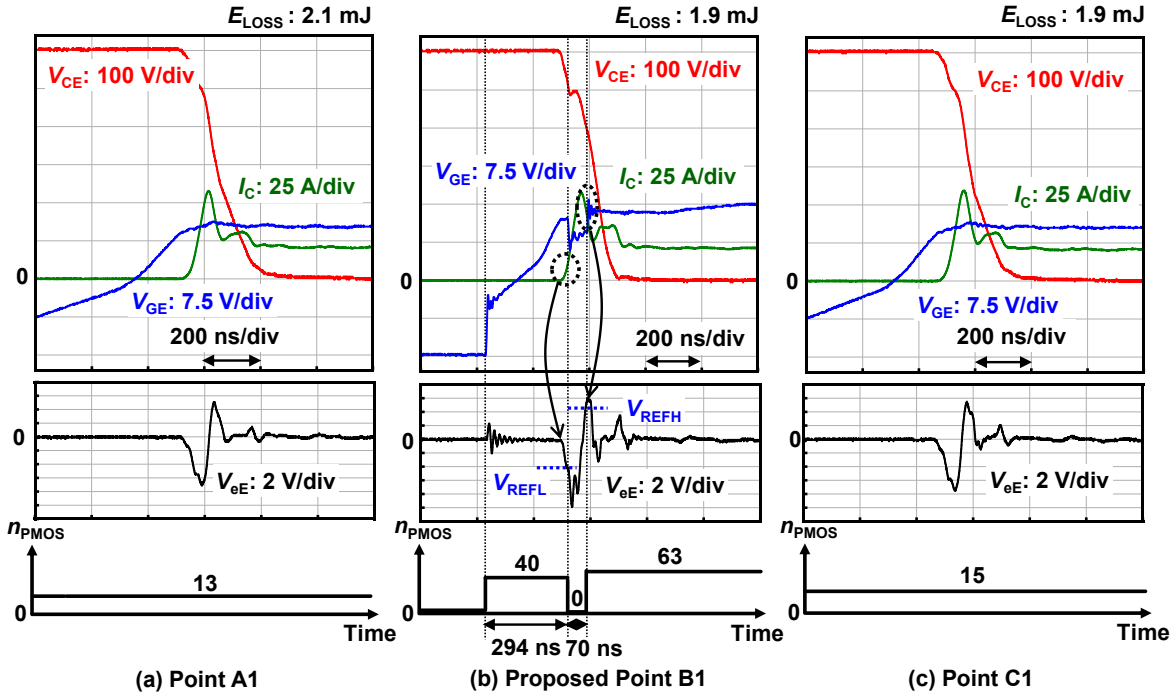

Fig. 12: Measured waveforms in Point A1, Proposed Point B1, and Point C1 in Fig. 10 (a) at I_L = 20 A and T_J = 25˚C.

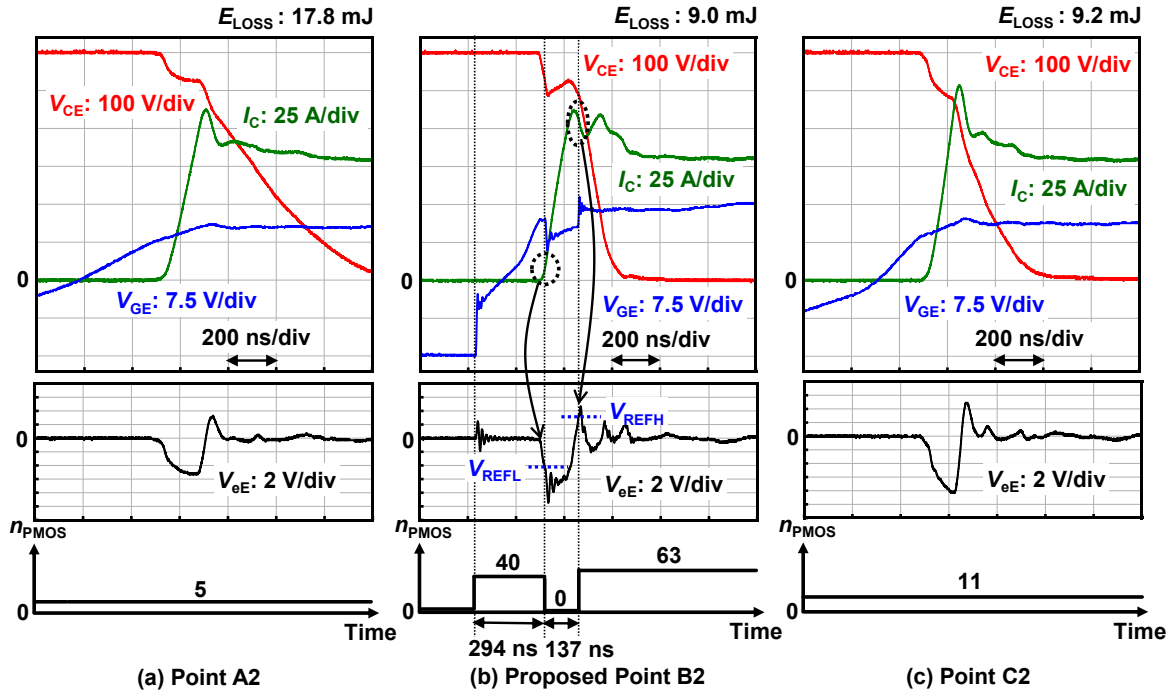

Fig. 13: Measured waveforms in Point A2, Proposed Point B2, and Point C2 in Fig. 10 (c) at I_L = 80 A and T_J = 25 ˚C.

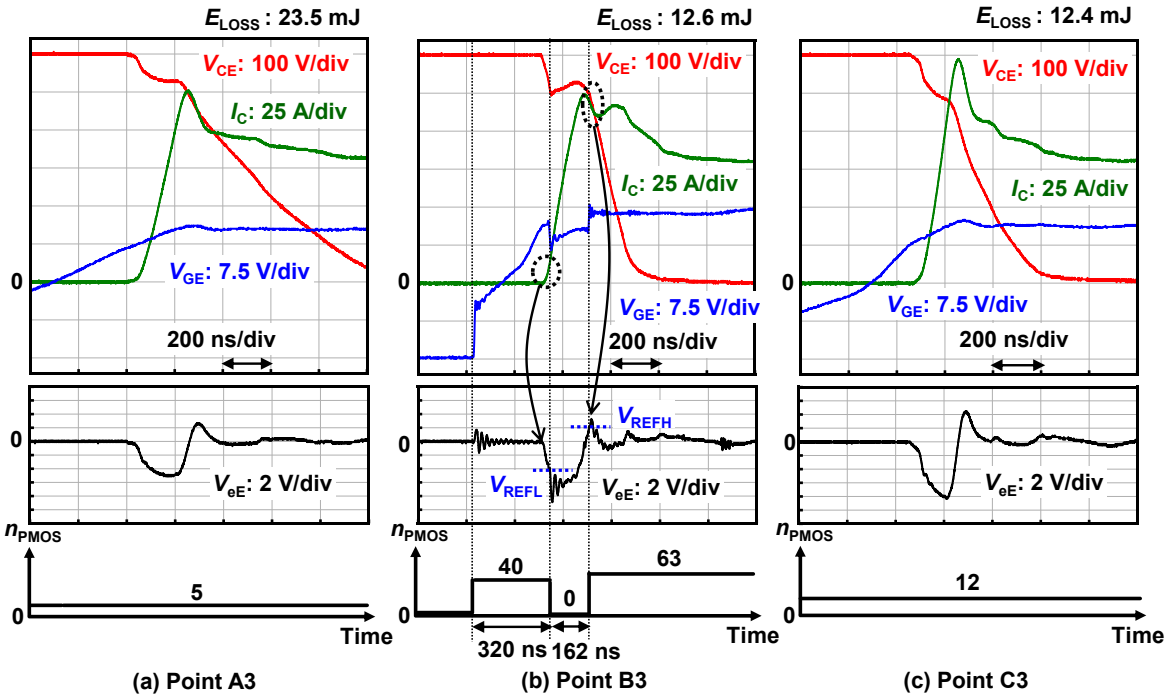

Fig. 14: Measured waveforms in Point A3, Proposed Point B3, and Point C3 in Fig. 10 (c) at I_L = 80 A and T_J = 125˚C.

SSGD (Point A2 and Point C2), the proposed SGGD (Point B2) reduces E_{LOSS} by 49 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 33 % under E_{LOSS}-aligned condition. At (I_L, T_J) = (80 A, 125 ˚C) in Fig. 10 (c), compared with the conventional SSGD (Point A3 and Point C3), the proposed SGGD (Point B3) reduces E_{LOSS} by 46 % under $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 34 % under E_{LOSS}-aligned condition.

Figs. 11 (a) to (c), on the other hand, show the measured E_{LOSS} vs. $I_{OVERSHOOT}$ of the conventional SSGD and the proposed SGGD at T_J = 25 ˚C, 75 ˚C, and 125 ˚C, respectively. In each graph, I_L is varied to 20 A, 50 A, and 80 A. Similarly, in each graph, The red curve, which represents I_L = 80 A, black curve, which represents I_L = 50 A, and blue curve, which represents I_L = 20 A, show the trade-off curves of the conventional SSGD with varied n_1 from 4 to 63, and the proposed SGGD has advantage over conventional SSGD on lower E_{LOSS} and lower $I_{OVERSHOOT}$.

Figs. 12 (a) to (c) show the measured waveforms in Point A1, which represents the waveform of SGGD with n_1 = 13, Point B1, the proposed SGGD, and Point C1, which represents the waveform of SGGD with n_1 = 15 in Fig. 10 (a), respectively, under I_L = 20 A, T_J = 25˚C condition. In Fig. 12 (b), SGGD is realized with t_1 and t_2 correctly controlled by detecting V_{eE} comparing to V_{REFH} and V_{REFL}. Figs. 13 (a) to (c) show the measured waveforms in Point A2, B2, and C2 in Fig. 10 (c), as SGGD with n_1 = 5, the proposed SGGD, and SGGD with n_1 = 11, respectively, under I_L = 80 A, T_J = 25˚C condition, regarded as the standard condition, commonly loaded by the IGBT device. Fig. 13 (b) clearly shows that the start of I_C flow and I_C overshoot are properly detected by V_{eE}. Similarly, Figs. 14 (a) to (c) show the measured waveforms in Point A3, B3, and C3, as SGGD with n1 = 5, the proposed SGGD, and SGGD with n_1 = 12, respectively, under I_L = 80 A, T_J = 125 ˚C condition. In Fig. 14 (b), automatic control of t_1 and t_2 has been successfully achieved by detecting V_{eE} comparing to V_{REFH} and V_{REFL}. Note also that comparing t_1 in Fig. 13 (b) and Fig. 14 (b), where T_J changed from 25 ˚C to 125 ˚C, t_1 increased from 294 ns to 320 ns. The T_J dependence of t_1 is successfully controlled automatically by the proposed ATC.

TABLE I. COMPARISON TABLE OF CLOSED-LOOP AGDS

	TPEL'15 [11]	TPEL'18 [12]	TPEL'21 [14]	ISSCC'19 [13]	ISSCC'21 [18]	This work
Target power device	IGBT	IGBT	SiC MOSFET	Si MOSFET	GaN FET	IGBT
Sensor input	dI_C/dt, V_{CE}	dI_C/dt, V_{CE}	dI_C/dt	V_{DS}	V_{DD} of high-side gate driver	dI_C/dt
Feedback control target	V_{GE} waveform	Timing of state change	Timing of state change	Timing of state change	Timing of state change	Timing of state change
Real-time control	Yes	Yes	Yes	No	No	Yes
Number of states per switching		4	3	3	3	3
Preset parameters for each state		I_G	V_{GS}	R_G	I_G	I_G
Levels of parameter		NA	2	2	3	6 bit
Implementation	PCB	PCB	PCB	IC (Not fully integrated)*	IC (Fully integrated)	IC (Fully integrated)
IC Process				130 nm HV CMOS	500 nm, 600 V SOI**	180 nm BCD

*Voltage divider for V_{DS} is not integrated.
**High-voltage IC process with the same breakdown voltage as V_{CC} of main circuit is required.

Table I shows a comparison table of the closed-loop AGDs. This paper is the first work achieving the fully integrated IC, the real-time control, and the programmable I_G in the closed-loop AGDs.

IV. CONCLUSIONS

The proposed DGD IC with ATC is the first work achieving the fully integrated IC, the real-time control, and the programmable I_G in the closed-loop AGDs. Low E_{LOSS} and low $I_{OVERSHOOT}$ can always be achieved at low cost even when the operating conditions, load current (I_L) and junction temperature (T_J), change. At I_L = 80 A and T_J = 25 ˚C,

compared with the conventional SSGD, SGGD with ATC using proposed DGD IC reduces E_{LOSS} by 49 % under the $I_{OVERSHOOT}$-aligned condition and reduces $I_{OVERSHOOT}$ by 33 % under the E_{LOSS}-aligned condition by automatically controlling t_1 and t_2 in real-time.

ACKNOWLEDGMENT

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